* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0010]
[Field of the Invention] This invention relates to the actuation circuit which drives the signal line of the liquid crystal display which performs a multi-gradation display.
[0020]
[Description of the Prior Art] The liquid crystal display (TFT-LCD) of a thin film transistor (TFT) mold is one of typical things of a liquid crystal display (Liquid Crystal Display).
[0030] The configuration of full color TFT-LCD of an active matrix is typically shown in drawing 8 . The TFT-liquid-crystal panel 100 which this kind of TFT-LCD carried out crisscross arrangement of two or more signal lines X1 and X2 and -- to two or more gate lines Y1 and Y2 and -- at the shape of a matrix, and has arranged the thin film transistor TFT to the pixel of each crossing, The gate line drivers G1 and G2 and -- to which parallel connection of [for driving the gate lines Y1 and Y2 of this liquid crystal panel 100 and --] was carried out, The signal-line (source) drivers S1 and S2 and -- to which parallel connection of [for driving the signal lines X1 and X2 of a liquid crystal panel 100 and --] was carried out, the controller 102 which controls actuation of each part, and the picture signal processing circuit 104 which performs necessary signal processing to the picture signal which should be displayed -- being full color (multi-gradation display) -- it consists of gradation electrical-potential-difference generating circuits 106 which generate the electrical potential difference of the many gradation for realizing.
[0040] The picture signal processing circuit 104 supplies digital image data DX showing the gradation of a display of each pixel to each signal-line drivers S1 and S2 and --. For example, in the case of 64 gradation, 6 bits [per each pixel of R, G, and B] image data DX is given to each signal-line drivers S1 and S2 and -- from the picture signal processing circuit 104. A controller 102 is Horizontal Synchronizing signal HS. And Vertical Synchronizing signal VS Various control signals or timing signals which synchronized are supplied to each gate line drivers G1 and G2, -- and each signal-line drivers S1 and S2, and --. The gradation electrical-potential-difference generating circuit 106 supplies the gradation electrical potential difference of the multistage story which has a voltage level corresponding to the many gradation of a display based on the V(electrical potential difference)-T (transmission) property of a liquid crystal panel 100, respectively to each signal-line drivers S1 and S2 and --.
[0050] The typical configuration of a liquid crystal panel 100 is shown in drawing 9 . It encloses or fills up with liquid crystal 114 between two glass substrates 110,112. One pixel electrode Pi and j which consists of transparence electric conduction film near the crossing location of each gate line Yi (not shown) and each signal line Xj (not shown) in the medial surface of one glass substrate 110 One thin film transistor TFTi and j It is formed. Pixel electrodes Pi and j TFTi and j It minds and is a signal line Xj. It connects and they are TFTi and j. The gate electrode Tg is the gate line Yi. It connects. The opposite (common) electrode 116 which becomes the medial surface of the glass substrate 112 of another side from the transparence electric conduction film through the light filter 115 of R (red), G

(green), and B (blue) is formed in the whole surface. As the lateral surface of both the glass substrates 110,112 and each deflection shaft are made to be parallel or cross at right angles mutually, the deflecting plate 118,120 is formed.

[0060] In addition, for a drain electrode and 124, as for a protective coat and 128, in drawing 9 , a semi-conductor layer and 126 are [Ts / a source electrode and Td / gate dielectric film and 130] black matrices.

[0070] The circuitry in a liquid crystal panel 100 is shown in drawing 10 . Each pixel electrodes Pi and j The signal storage capacitance Cs for 1 pixel is constituted by the liquid crystal 114 inserted between a counterelectrode 116 and both. The gate lines Y1 and Y2 and .... of one line are usually chosen at a time by the gate line drivers G1 and G2 and -- by line sequential scanning within an one-frame period, and are driven to an active state.

[0080] Now and gate line Yi of i lines If it drives, it is this gate line Yi. All thin film transistor TFTi(s) of i lines connected, 1, TFTi, 2, and .... turn on. Synchronizing with this, the gradation electrical potential difference of the analog to all the pixels on i lines is outputted from the signal-line drivers S1 and S2 and --, respectively, and these gradation electrical potential differences are impressed to signal lines X1 and X2, ... and thin film transistor TFTi of an ON state, 1, TFTi, 2, the pixel electrode Pi that corresponds through .., respectively, 1, Pi, 2, and --. Then, it sets in the following line (i+1), and is gate line Yi+1. It is chosen and the same actuation as the above is performed. In i lines, it is that thin film transistor TFTi, 1, TFTi, 2, and .... are turned off, and as for the charge written in each pixel, a recess path is lost, and each electrode Pi, 1, Pi, 2, and the gradation electrical potential difference of -- are held to the following selection time amount.

[0090] Thus, although a gradation electrical potential difference is impressed to each pixel electrode with 1 frame period, with a liquid crystal display, an electrical potential difference must be impressed to liquid crystal with the gestalt of an alternating current for degradation prevention of a liquid crystal molecule. In TFT-LCD, there are the so-called common fixed driving method and the common reversal driving method in the approach of impressing alternating voltage to liquid crystal.

[0100] The common fixed driving method impresses by turns the electrical potential difference which has a forward polarity to a counterelectrode electrical potential difference (constant value) in a pixel electrode, fixing the electrical potential difference of a counterelectrode to fixed level as shown in drawing 11 , and the electrical potential difference which has a negative polarity.

[0110] The common reversal driving method impresses by turns the electrical potential difference which has a forward polarity to a counterelectrode electrical potential difference in a pixel electrode, and the electrical potential difference which has a negative polarity, reversing the electrical potential difference of a counterelectrode between a high level and a low, as shown in drawing 12 . In this case, when the electrical potential difference of a counterelectrode is a high level, the electrical potential difference which has a negative polarity on the basis of this high level is impressed to a pixel electrode, and when the electrical potential difference of a counterelectrode is a low, the electrical potential difference which has a forward polarity on the basis of this low will be impressed to a pixel electrode.

[0120] Although there is an advantage that a low-battery driver can be used since the common reversal driving method can be managed with one half compared with the case where the voltage swing of a pixel electrode is the common fixed driving method, in order to carry out alternating current actuation of the mass counterelectrode, dot reversal in the direction of X cannot be performed a top with much power consumption, but there is a fault which is inferior also in respect of display quality. While a low-battery driver cannot be used for the common fixed driving method, objection has little power consumption and not only the direction of Y but dot reversal in the direction of X is more possible for it than the common reversal driving method to it, and it excels in display quality at it. From such a thing, it is said that the common fixed driving method is especially suitable by TFT-LCD of a big screen.

[0130] The pattern of perfect dot reversal is shown in drawing 13 . Like a graphic display, whenever Frame F changes, the polarity of the gradation electrical potential difference written in each pixel in (Fn, Fn+1), and a liquid crystal panel 100 every is reversed by turns. And a polarity is [both] reversed also in the direction of X for every pixel in if the polarity of each pixel is reversed for every line in the

direction of Y.
[0140] By the common reversal driving method, the polarity of the gradation electrical potential difference in each pixel can be reversed with a frame period and a line period (the direction of Y) according to making a frame period and a line period reverse the level of a counterelectrode electrical potential difference. However, in a point, a signal line can be driven only with the polarity of straight polarity or one of negative polarity to a counterelectrode electrical potential difference temporarily. For this reason, a gradation electrical potential difference can be impressed to the pixel for one line which will be in an ON state simultaneously only with the polarity of straight polarity or one of negative polarity, and the polarity of a gradation electrical potential difference cannot be reversed for every pixel in the direction of X.
[0150] On the other hand, since the gradation electrical potential difference of straight polarity and negative polarity can be simultaneously chosen at the event of arbitration by the common fixed driving method, in view of a counterelectrode electrical potential difference, as shown in drawing 1313 , it is possible to reverse a polarity by turns for every pixel about all the pixels in a liquid crystal panel 100 not only in a frame period and the direction of Y but in the direction of X. Thus, at the time of writing, the current which flows with a counterelectrode etc. negates each other into next doors, and deterioration of display quality is suppressed by this because the polarity of a gradation electrical potential difference is reversed with a ****** signal line thru/or a pixel electrode.
[0160]
[Problem(s) to be Solved by the Invention] When performing perfect dot reversal in the above common fixed driving methods, it is each signal line Xj. A polarity reverses the upper actuation (gradation) electrical potential difference by turns by the same wave as drawing 11 R> 1 for every 1 horizontal-scanning period. In this case, a horizontal scanning period changes and the signal-line driver S is sometimes each signal line Xj. By making a counterelectrode electrical potential difference into criteria (core), from one polar gradation electrical potential difference, as it shakes to the polar gradation electrical potential difference of another side, it drives to it.
[0170] Such a signal line Xj The upper electrical-potential-difference swing width is this signal line Xj. It is proportional to the sum of the display gradation of the pixel which gets mixed up in a top (the direction of Y) (******). When all of the pixel which follows, for example, gets mixed up have the maximum display gradation, it is a signal line Xj to the maximum gradation electrical potential difference of the maximum gradation electrical potential difference of straight polarity (or negative polarity) to negative polarity (or straight polarity). A full swing must be made to take for the upper electrical potential difference. For this reason, the signal-line driver S will consume power so much, in having to have big actuation capacity.
[0180] From now on, a liquid crystal display can ask for low-power-ization increasingly. Also in it, the demand of low-power-izing to a signal-line driver is still stronger.
[0190] This invention was made in view of the trouble of this conventional technique, and aims at offering the signal-line actuation circuit for liquid crystal displays which enabled it to perform dot reversal actuation of the common fixed driving method by the low-power method.
[0200] Furthermore, this invention aims at offering the signal-line actuation circuit for liquid crystal displays which realizes low-power-ization in dot reversal actuation of the common fixed driving method with a simple mechanism.
[0210]
[Means for Solving the Problem] In order to attain the above-mentioned object, it fills up with liquid crystal between two or more pixel electrodes and one counterelectrode with which this invention has been arranged in the shape of a matrix. While each the electrode of said pixel is electrically connected to the signal line which each corresponds through the thin film transistor which each corresponds The control terminal of said thin film transistor is electrically connected to the gate line which each corresponds. A predetermined counterelectrode electrical potential difference is impressed to said counterelectrode, and whenever said gate line which each corresponds to each the electrode of said pixel drives, it has a voltage level corresponding to the display gradation of the request to every. And it sets in

the signal-line actuation circuit for liquid crystal displays constituted so that the gradation electrical potential difference which has a polarity polar [forward] or negative relatively to said counterelectrode electrical potential difference might be impressed through said signal line and said thin film transistor. The 1st actuation which supplies the gradation electrical potential difference of negative polarity to each signal line of an even number train at the same time it supplies the gradation electrical potential difference of straight polarity to each signal line of an odd number train, The means for switching which makes each signal line of an even number train repeat by turns the 2nd actuation which supplies the gradation electrical potential difference of straight polarity with a predetermined period at the same time it supplies the gradation electrical potential difference of negative polarity to each signal line of an odd number train, It has the short-circuiting means which short-circuits temporarily the signal lines of the odd number train of arbitration, and an even number train to predetermined timing at the time of the change-over between said 1st actuation and said 2nd actuation.

[0220] As one desirable embodiment of this invention, said switching means is made into an open condition at the time of the switching means by which said short-circuiting means was connected between the signal lines of each ****** couple, and a stationary, and it has the switch control means to which only the period which supply of the gradation electrical potential difference to each signal line interrupts at the time of said change-over makes said switching means a closed state.

[0230] Or as another embodiment, said switching means is made into an open condition at the time of the switching means by which said short-circuiting means was connected among all ****** signal lines, and a stationary, and it has the switch control means to which only the period which supply of the gradation electrical potential difference to each signal line interrupts at the time of said change-over makes said switching means a closed state.

[0240] As other embodiments, said short-circuiting means has the connecting means which connects each signal line to the voltage source which gives an electrical potential difference almost equal to said counterelectrode electrical potential difference during the period when said switching means is a closed state electrically.

[0250] Moreover, said means for switching makes said the 1st actuation and said actuation of the 2nd repeat by turns as one desirable embodiment of this invention with the frame period with which said gradation electrical potential difference is impressed to each the electrode of said pixel while said gate line makes said the 1st actuation and said actuation of the 2nd repeat by turns with the line period driven by line sequential scanning, or the period of the integral multiple.

[0260] Moreover, it fills up with liquid crystal between two or more pixel electrodes and one counterelectrode with which the liquid crystal display of this invention has been arranged in the shape of a matrix. While each the electrode of said pixel is electrically connected to the signal line which each corresponds through the thin film transistor which each corresponds The liquid crystal panel by which the control terminal of said thin film transistor was electrically connected to the gate line which each corresponds, A means to impress a fixed counterelectrode electrical potential difference to said counterelectrode, and the gate line driving means which activates said gate line in order by line sequential scanning, It has a voltage level corresponding to desired display gradation to said pixel electrode which corresponds every whenever each the line of said gate is activated. And the signal-line driving means which impresses the gradation electrical potential difference which has a polarity polar [forward] or negative relatively to said counterelectrode electrical potential difference through said signal line, The 1st actuation which supplies the gradation electrical potential difference of negative polarity to each signal line of an even number train at the same time said signal-line driving means supplies the gradation electrical potential difference of straight polarity to each signal line of an odd number train, The means for switching which makes each signal line of an even number train repeat by turns the 2nd actuation which supplies the gradation electrical potential difference of straight polarity with a predetermined period at the same time said signal-line driving means supplies the gradation electrical potential difference of negative polarity to each signal line of an odd number train, It has the short-circuiting means which short-circuits temporarily the signal lines of the odd number train of arbitration, and an even number train to predetermined timing at the time of the change-over between

said 1st actuation and said 2nd actuation.
[0270]
[The mode of implementation of invention] Hereafter, the example of this invention is explained with reference to drawing 1 - drawing 7 .
[0280] Drawing 1 shows the circuitry of the important section of the signal-line driver by one example of this invention, and shows the configuration of the actuator for the channel of each two ****** more to a detail. This signal-line driver may be used for full color TFT-LCD of the active matrix shown in drawing 8 . In addition, the actuator for the channel of two ****** of a graphic display is the signal line Xj of the j-th train of ****** of the liquid crystal panel 100 shown in drawing 8 R> 8, and a ** (j+1) train, and Xj+1. It shall drive.
[0290] In drawing 1 the actuator for the channel of each two ****** The registers 10L and 10R of a couple, the 1st data latch circuits 12L and 12R of a couple, The 1st change-over circuits 14L and 14R of a couple, the 2nd data latch circuits 16L and 16R of a couple, It consists of the level shifters 18L and 18R of a couple, DA converters 20L and 20R of a couple, output amplifier 22L and 22R of a couple, 2nd change-over circuits 24L and 24R of a couple, and output pads 26L and 26R of a couple.
[0300] The registers 10L and 10R of left-hand side and right-hand side are the image data DXj for 1 pixel assigned to the channel which is one line (horizontal scanning period) in a predetermined period, for example, period, and each corresponds from the picture signal processing circuit 104 (drawing 8), and DXj+1. It incorporates, respectively. And it is the image data DXj for these 1 pixels, and DXj+1 from both the registers 10L and 10R at predetermined timing. It is latched to the 1st data latch circuits 12L and 12R of left-hand side and right-hand side, respectively.
[0310] The output terminal of left-hand side 1st data latch circuit 12L is connected to the input terminal of another side (right-hand side) of right-hand side 1st change-over circuit 14R while connecting with the input terminal [on the other hand / (left-hand side)] of left-hand side 1st change-over circuit 14L for every bit. For every bit, the output terminal of right-hand side 1st data latch circuit 12R is connected to the input terminal of another side (right-hand side) of left-hand side 1st change-over circuit 14L while connecting with the input terminal [on the other hand / (left-hand side)] of right-hand side 1st change-over circuit 14R.
[0320] The 1st change-over circuits 14L and 14R of left-hand side and right-hand side are switched to an input terminal [on the other hand / (every 1 horizontal-scanning period) / (left-hand side)] and the input terminal of another side (right-hand side) by turns for example, in a cycle of one line by the alternating current-ized signal or the polar change-over signal REV from a controller 102 (drawing 8). The output terminal of the 1st change-over circuits 14L and 14R of left-hand side and right-hand side is connected to the input terminal of the 2nd data latch circuits 16L and 16R of left-hand side and right-hand side, respectively.
[0330] The 2nd data latch circuits 16L and 16R of left-hand side and right-hand side incorporate [with the data latch control signal TP from the controller 102 which synchronized with the alternating current-ized signal REV] the image data for 1 pixel through the 1st change-over circuits 14L and 14R of left-hand side and right-hand side from either left-hand side 1st data latch circuit 12L or right-hand side 1st data latch circuit 12R to the timing of every 1 horizontal-scanning period. The output terminal of the 2nd data latch circuits 16L and 16R of left-hand side and right-hand side is connected to the input terminal of DA converters 20L and 20R of left-hand side and right-hand side through the level shifters 18L and 18R of left-hand side and right-hand side, respectively.
[0340] Level shifters 18L and 18R transform the logic electrical potential difference (for example, 5V) of image data into a high electrical potential difference (for example, 10V) so that the circuit element in DA converter20L and 20R can treat the gradation electrical potential difference covering the both sides of the straight polarity by the common fixed driving method, and negative polarity.
[0350] In left-hand side DA converter20L, it is gradation electrical-potential-difference V1 -VK of all the straight polarity (K pieces) from the gradation electrical-potential-difference generating circuit 28. It is supplied. On the other hand, gradation electrical-potential-difference V'K-V'1 of all the negative polarity (K pieces) is supplied to right-hand side DA converter20R from the gradation electrical-

potential-difference generating circuit 28.
[0360] The gradation electrical-potential-difference generating circuit 28 consists for example, of a resistance partial pressure circuit, and the reference voltage v for amendment is supplied at the node (node) of a suitable part so that each gradation electrical potential difference which has a voltage level corresponding to each display gradation according to the V-T property of a liquid crystal panel 100 may be obtained.
[0370] For example, it sets by the common fixed driving method, and is the electrical potential difference VCOM of a counterelectrode. It fixes to 5 volts. When the gradation electrical potential difference (5-10 volts) of straight polarity and the gradation electrical potential difference (5-0 volt) of negative polarity are impressed to each pixel electrode by turns, The maximum gradation electrical potential difference VK of straight polarity It is set as the value nearest to 10 volts, maximum gradation electrical-potential-difference V'K of negative polarity is set as the value nearest to 0 volt, and the minimum gradation electrical potential difference V1 of amphipathy and V'1 are set up near 5 volt.
[0380] Left-hand side DA converter 20L is the gradation electrical potential difference Vx of the straight polarity which has a voltage level corresponding to the display gradation with which the image data for 1 pixel inputted from left-hand side level-shifter 18L is decoded, and the image data expresses. It chooses, and it is constituted so that it may output. On the other hand, right-hand side DA converter 20R decodes the image data for 1 pixel inputted from right-hand side level-shifter 18R, and it is constituted so that gradation electrical-potential-difference V'x of the negative polarity which has a voltage level corresponding to the display gradation with which the image data expresses may be chosen and outputted. The output terminal of DA converters 20L and 20R of left-hand side and right-hand side is connected to the input terminal of the output amplifier 22L and 22R of left-hand side and right-hand side, respectively.
[0390] Left-hand side output amplifier 22L consists of an electrical-potential-difference follower of the operational amplifier which has an impedance-conversion function, and it is constituted so that it may operate in the state of a sink within the limits of a straight polarity electrical potential difference. The output terminal of output amplifier 22L of this left-hand side is connected to the input terminal of another side (right-hand side) of right-hand side 2nd change-over circuit 24R while connecting with the input terminal [on the other hand / (left-hand side)] of left-hand side 2nd change-over circuit 24L.
[0400] Right-hand side output amplifier 22R consists of an electrical-potential-difference follower of the operational amplifier which has an impedance-conversion function, and it is constituted so that it may operate in the state of the source within the limits of a negative polarity electrical potential difference. The output terminal of output amplifier 22R of this right-hand side is connected to the input terminal of another side (right-hand side) of left-hand side 2nd change-over circuit 24L while connecting with the input terminal [on the other hand / (left-hand side)] of right-hand side 2nd change-over circuit 24R.
[0410] Each 2nd change-over circuits 24L and 24R switch with the change-over control signal SW generated from the change-over control circuit 32 based on the alternating current-ized signal REV and the data latch control signal TP.
[0420] The output terminal of the 2nd change-over circuits 24L and 24R of left-hand side and right-hand side is electrically connected to the signal line Xj of a channel (train) which each corresponds through the output pads 26L and 26R of left-hand side and right-hand side, respectively, and Xj+1 (not shown in drawing 1). Both the output pads 26L and 26R thru/or both the signal lines Xj, and Xj+1 In between, the open/close switch 30 is connected.
[0430] This open/close switch 30 is opened and closed with the closing motion control signal SH given from the change-over control circuit 32. The signal line Xj and Xj+1 which adjoin each other through this switch 30 and the output pads 26L and 26R if this switch 30 will be in a close (flow) condition Comrades connect too hastily electrically.
[0440] Next, actuation of the signal-line driver by this example is explained. The wave (an example) of the signal of each part in the case of performing perfect dot reversal to drawing 2 is shown.
[0450] In TFT-LCD containing this signal-line driver, the gate lines Y1 and Y2 of a liquid crystal panel 100 and .... are usually chosen by the gate line drivers G1 and G2 and -- one line (line) every by line

sequential scanning within an one-frame period, and it drives to an active state. Whenever each gate line Y drives, in each signal-line driver, the gradation electrical potential difference V which should be impressed to a pixel electrode [on the line concerned / each] from the output pad 26 of each channel is outputted.
[0460] Now and gate line Yi of i lines When driving, the logical value of the alternating current-ized signal REV presupposes that each 1st change-over circuits 14L and 14R and each 2nd change-over circuits 24L and 24R have switched to the input terminal [on the other hand / (left-hand side) / respectively] by L. the image data DXi and j which expresses the display gradation of two pixels located in the i line j train and i line (j+1) train in a liquid crystal panel 100, respectively from the 1st data latch circuits 12L and 12R at this time, DXi, and j+1 It is inputted into DA converters 20L and 20R of left-hand side and right-hand side through the 1st change-over circuits 14L and 14R, the 2nd data latch circuits 16L and 16R, and level shifters 18L and 18R, respectively.
[0470] Thereby, from left-hand side DA converter20L, it is image data DXi and j. Gradation electrical potential difference Vj of the straight polarity which has a voltage level corresponding to the display gradation with which it expresses It is outputted. On the other hand, from right-hand side DA converter20R, it is image data DXi and j+1. Gradation electrical-potential-difference V'j +1 of the negative polarity which has a voltage level corresponding to the display gradation with which it expresses is outputted.
[0480] Gradation electrical potential difference Vj of the straight polarity outputted from left-hand side DA converter 20L Left-hand side output amplifier 22L and 2nd change-over circuit 24L are minded, and it is the signal line Xj of j train from left-hand side output pad 26L. It is outputted. On the other hand, gradation electrical-potential-difference V'j +1 of the negative polarity outputted from right-hand side DA converter 20R minds right-hand side output amplifier 22R and 2nd change-over circuit 24R, and is signal-line Xj+1 of a train (j+1) from right-hand side output pad 26R. It is outputted.
[0490] under the present circumstances, left-hand side output amplifier 22L -- signal line Xj of j train Counterelectrode electrical potential difference VCOM Gradation electrical potential difference Vj of near corresponding medium level to straight polarity up to -- driving -- ****ing -- right-hand side output amplifier 22R -- signal-line Xj+1 of a train (j+1) What is necessary is just to drive from near medium level (VCOM) to gradation electrical-potential-difference V'j +1 of negative polarity.
[0500] In this way, each signal line Xj and Xj+1 After potential reaches the desired gradation electrical potential difference Vj and V'j +1, respectively, the gate line Yi of i lines is activated by H level by the gate line driver G to predetermined timing, and it is this gate line Yi. All thin film transistor TFTi(s) of i lines connected, 1, TFTi, 2, and .... are turned on. Thereby, it is the signal line Xj of j train. Gradation electrical potential difference Vj of straight polarity Thin film transistor TFTi and j are minded and they are the pixel electrodes Pi and j of an i line J train. It is written in and is signal-line Xj+1 of a train (j+1). Gradation electrical-potential-difference V'j +1 of negative polarity minds thin film transistor TFTi and j+1, and it is the pixel electrode Pi of an i line (j+1) train, and j+1. It is written in.
[0510] Next, gate line Yi+1 of a line (i+1) The data latch control signal TP starts on H level from L level at the same time the logical value of the alternating current-ized signal REV is reversed from L to H at the time of initiation of the horizontal scanning period, when driving.
[0520] By the logical value of the alternating current-ized signal REV being set to H, the 1st change-over circuits 14L and 14R switch to the input terminal of another side (right-hand side), respectively. It follows for starting. and H level of the data latch control signal TP -- It is the signal line Xj of j train from left-hand side 1st data latch circuit 12L. Image data DXi+1 for 1 pixel corresponding and j At the same time it is transmitted to right-hand side 2nd data latch circuit 16R through right-hand side 1st change-over circuit 14R It is signal-line Xj+1 of a train (j+1) from right-hand side 1st data latch circuit 12R. Image data DXi+1 for 1 pixel corresponding and j+1 corresponding It is transmitted to left-hand side 2nd data latch circuit 16L through left-hand side 1st change-over circuit 14L.
[0530] On the other hand, synchronizing with the standup of the above data latch control signals TP, the 2nd change-over circuits 24L and 24R will be in a cut off state with the change-over control signal SW from the change-over control circuit 32. thereby -- both the output amplifier 22L and 22R -- the output

pads 26L and 26R thru/or a signal line Xj, and Xj+1 from -- it is intercepted electrically.
[0540] In this case, since the logical value of the alternating current-ized signal REV is reversed synchronizing with the standup of the data latch control signal TP, while the 2nd change-over circuits 24L and 24R are cuts off state as mentioned above, an open/close switch 30 will be in switch-on with the closing motion control signal SH from the change-over control circuit 32. The signal line Xj which adjoins each other by this through the switch 30 and the output pads 26L and 26R of this switch-on, and Xj+1 Comrades connect too hastily mutually.
[0550] Signal line Xj of during the last horizontal scanning period and j train It is the gradation electrical potential difference Vj of straight polarity from left-hand side DA converter 20L. Electric power is supplied and it is signal-line Xj+1 of a train (j+1). It is gradation electrical-potential-difference Vj+1 of negative polarity from right-hand side DA converter 20R. Electric power is supplied. Therefore, it is at the polarity-reversals time of alternating-current-izing, and is both the signal lines Xj and Xj+1 at the time of initiation of a horizontal scanning period. By connecting too hastily mutually through a switch 30, it is both the signal lines Xj and Xj+1. The upper potential is negated mutually and equalized near reference level (VCOM), respectively.
[0560] If the data latch control signal TP falls from H level to L level, they are image data DXi+1 for 1 pixel, j+1, DXi+1, and j from the 2nd data latch circuits 16L and 16R of left-hand side and right-hand side. It is inputted into DA converters 20L and 20R of left-hand side and right-hand side through the level shifters 18L and 18R of left-hand side and right-hand side, respectively.
[0570] Thereby, from left-hand side DA converter20L, it is image data DXi+1 and j+1. Gradation electrical-potential-difference Vj+1 of straight polarity which has a voltage level corresponding to the display gradation with which it expresses It is outputted. On the other hand, from right-hand side DA converter20R, they are image data DXi+1 and j. Gradation electrical-potential-difference V'j of the negative polarity which has a voltage level corresponding to the display gradation with which it expresses is outputted.
[0580] On the other hand, when the data latch control signal TP falls from H level to L level as mentioned above, an open/close switch 30 switches to an open condition by control of the change-over control circuit 32 at this and coincidence, and the 2nd change-over circuits 24L and 24R switch to the input terminal of another side (right-hand side), respectively.
[0590] By a switch 30 being in an open condition, it is both the signal lines Xj and Xj+1. It is intercepted electrically. Moreover, the output terminal of left-hand side output amplifier 22L is connected to right-hand side output pad 26R through right-hand side 2nd change-over circuit 24R, and the output terminal of right-hand side output amplifier 22R is connected to left-hand side output pad 26L through left-hand side 2nd change-over circuit 24L because the 2nd change-over circuits 24L and 24R switch to the input terminal of another side (right-hand side), respectively.
[0600] gradation electrical-potential-difference Vj+1 of the straight polarity outputted from left-hand side DA converter 20L by this Left-hand side output amplifier 22L and right-hand side 2nd change-over circuit 24R are minded, and it is signal-line Xj+1 of a train (j+1) from right-hand side output pad 26R. It is outputted. This signal-line Xj+1 Thin film transistor TFTi+1 of the line connected (i+1), and j+1 Pixel electrode Pi+1 and j+1 which mind and correspond It is impressed.
[0610] On the other hand, gradation electrical-potential-difference V'j of the negative polarity outputted from right-hand side DA converter 20R minds right-hand side output amplifier 22R and left-hand side 2nd change-over circuit 24L, and is the signal line Xj of j train from left-hand side output pad 26L. It is outputted and is this signal line Xj. Thin film transistor TFTi+1 of the line connected (i+1), and j Pixel electrode Pi+1 and j which mind and correspond It is impressed.
[0620] in this case, left-hand side output amplifier 22L -- signal-line Xj+1 of a train (j+1) Gradation electrical-potential-difference Vj+1 of near medium level (VCOM) to straight polarity up to -- driving -- ****ing -- right-hand side output amplifier 22R -- signal line Xj of j train What is necessary is just to drive from near medium level (VCOM) to gradation electrical-potential-difference V'j of negative polarity.
[0630] In this way, each signal line Xj and Xj+1 After potential amounts to desired gradation electrical-

potential-difference V'j and Vj+1, respectively predetermined timing -- the gate line driver G -- gate line Yi+1 of a line (i+1) it is activated on H level -- having -- this gate line Yi+1 all thin film transistor TFTi+ of the line connected (i+1) -- 1, 1, and TFTi+ -- 1, 2, and .... are turned on. By this, it is the signal line Xj of j train. Gradation electrical-potential-difference V'j of negative polarity is thin film transistor TFTi+1 and j. It minds and they are pixel electrode Pi+1 of a line (i+1) J train, and j. It is written in. (j+1) Signal-line Xj+1 of a train Gradation electrical-potential-difference Vj+1 of straight polarity It is written in pixel electrode Pi+1 of a line (i+1) (j+1) train, and j+1 through thin film transistor TFTi+1 and j+1.

[0640] In addition, gate line Yi of i lines An open/close switch 30 flows during the period to which the closing motion control signal SH has H level at the time of initiation of the horizontal scanning period even when driving, and it is both the signal lines Xj and Xj+1. It connects too hastily mutually and is both the above signal lines Xj and Xj+1. The denial of the potential of a between or equalization is performed.

[0650] Henceforth, the above-mentioned actuation for two lines is repeated. Thereby, in the direction of Y of a liquid crystal panel 100, the polarity of a gradation electrical potential difference is reversed for every pixel. Moreover, also in the direction of X, the polarity of a gradation electrical potential difference is reversed for every pixel (between two each adjoining signal lines Xj and Xj+1).

[0660] in addition, each change-over circuits 14L, 14R, 24L, and 24R switch for every frame with the alternating current-ized signal REV (namely, the location of each change-over circuits 14L, 14R, 24L, and 24R in case the gate line Yi of each line drives is reversed for every frame) -- it is controlled like. The electrode voltage wave by the common fixed driving method as shown in drawing 11 is acquired by reversal of such a frame period.

[0670] As described above, in the signal-line driver by this example In the actuator for the channel of each two ******, while constituting [of straight polarity] left-hand side DA converter20L and output amplifier 22L only on gradation electrical potential differences, right-hand side DA converter20R and output amplifier 22R are only constituted [of negative polarity] on gradation electrical potential differences. By switching the 1st change-over circuits 14L and 14R established in the preceding paragraph of both DA converters 20L and 20R, and the 2nd change-over circuits 24L and 24R established in the latter part of both the output amplifier 22L and 22R with a predetermined period, for example, the period of one line, and a predetermined frame period Perfect dot reversal (reversal in every pixel) as shown in the common fixed driving method as shown in drawing 11 , and drawing 13 is realized.

[0680] each output amplifier 22L and 22R -- the range of polar gradation electrical potential difference of one of the two -- always -- either a sink condition or a source condition -- operating -- ****ing -- especially -- up to the gradation electrical potential difference of a polar request of near medium level (VCOM) to one of the two at the time of the polarity reversals of alternating-current-izing -- a signal line Xj and Xj+1 driving -- ****ing -- electrical-potential-difference swing width -- the former -- it ends with one half mostly. For this reason, power consumption is reduced substantially.

[0690] Moreover, in each output amplifier 22L and 22R, since actuation capacity is small and ends, while the circuit magnitude for one channel becomes small, properties, such as a dynamic range or linearity, and offset, also improve.

[0700] In addition, it is possible to choose an alternating current-ized period as arbitration. The wave (an example) of the signal of each part in the case of making drawing 3 reverse the polarity of the gradation electrical potential difference written in the pixel of each train (the direction of Y) in a cycle of two line (2 horizontal-scanning period) is shown.

[0710] As shown in drawing 3 , the closing motion control signal SH is activated to the same timing as the data latch control signal TP, when the logical value of the alternating current-ized signal REV is reversed. That is, when the polarity of an electrical potential difference is reversed on each signal line X, an open/close switch 30 closes, and it is each ****** signal line Xj and Xj+1. Comrades are short-circuited. By this, as the potential of each signal line X is negated mutually as the potential of the reversed polarity of the next signal line, it will be equalized near medium level (VCOM), and it will be

driven from the average level to the gradation electrical potential difference of a request of reversed polarity with the predetermined output amplifier 22.
[0720] In addition, in drawing 2 and drawing 3 , it sets on each [after / expedient / understanding it as explanation] line, and is the signal line Xj of j train. Signal-line Xj+1 of the gradation electrical potential difference given and a train (j+1) The gradation electrical potential difference given is mostly illustrated as an equal.
[0730] The 2nd change-over circuits 24L and 24R and the example of circuitry of an open/close switch 30 are shown in drawing 4 . this example of a configuration -- each 2nd change-over circuits 24L and 24R -- the transfer gate TGa of a couple, and TGb from -- becoming -- an open/close switch 30 -- the one transfer gate TGc from -- it becomes. the change-over control circuit 32 -- the transfer gate TGa of each 2nd change-over circuits 24L and 24R, and TGb **** -- the change-over control signal SWa and SWb it gives, respectively -- having -- the transfer gate TGc of an open/close switch 30 **** -- the closing motion control signal SH is given.
[0740] When the logical values of a change-over control signal [SWa and SWb] are [L, L], it sets in each 2nd change-over circuits 24L and 24R, and it is the left-hand side transfer gate TGa. It is ON and is the right-hand side transfer gate TGb. OFF comes. Thereby, the output terminal of left-hand side output amplifier 22L is the left-hand side transfer gate TGa of left-hand side 2nd change-over circuit 24L. It minds, and connects with left-hand side output pad 26L, and the output terminal of right-hand side output amplifier 22R is the left-hand side transfer gate TGa of right-hand side 2nd change-over circuit 24R. It minds and connects with right-hand side output pad 26R.
[0750] Reversely, when the logical values of a change-over control signal [SWa and SWb] are [H, H], it sets in each 2nd change-over circuits 24L and 24R, and it is the left-hand side transfer gate TGa. It is off and is the right-hand side transfer gate TGb. It becomes ON. Thereby, the output terminal of left-hand side output amplifier 22L is the right-hand side transfer gate TGb of right-hand side 2nd change-over circuit 24R. It minds, and connects with right-hand side output pad 26R, and the output terminal of right-hand side output amplifier 22R is the right-hand side transfer gate TGb of left-hand side 2nd change-over circuit 24L. It minds and connects with left-hand side output pad 26L.
[0760] Moreover, when the logical values of a change-over control signal [SWa and SWb] are [H, L], it sets in each 2nd change-over circuits 24L and 24R, and they are both the transfer gate TGa and TGb. Both become OFF. At this time, all of both the output amplifier 22L and 22R are intercepted from the output pads 26L and 26R.
[0770] At the time of a stationary, it is maintained at L and, thereby, the logical value of the closing motion control signal SH is the transfer gate TGc of an open/close switch 28. It is held at an OFF state. However, the closing motion control signal SH is set to H during the period, i.e., the period when the 2nd change-over circuits 24L and 24R are cuts off state, when the logical value of a change-over control signal [SWa and SWb] is [H, L], and it is the transfer gate TGc of an open/close switch 30. It is turned on. The signal line Xj which adjoins each other through this switch 30 and the output pads 26L and 26R as described above if it does so, and Xj+1 Comrades will connect too hastily electrically.
[0780] The example of circuitry of the change-over control circuit 30 is shown in drawing 5 . In this example of a configuration, while the closing motion control signal SH is generated by a delay circuit 34, an exclusive OR circuit 36, and the AND gate 38 based on the alternating current-ized signal REV and the data latch control signal TP, based on this closing motion control signal SH and the alternating current-ized signal REV, the change-over control signal SW (SWa and SWb) is generated by an inverting circuit 42, the OR gate 40, and the AND gate 44.
[0790] That is, when the logical value of the alternating current-ized signal REV is reversed from H to L or its reverse, the pulse signal of a logical value H is obtained by the output terminal of an exclusive OR circuit 36. The pulse width of this pulse signal is equivalent to the time delay in a delay circuit 34, and may be chosen as a usually bigger value than the pulse width of the data latch control signal TP.
[0800] The data latch control signal TP is given synchronizing with the alternating current-ized signal REV. When the logical value of REV is reversed in a cycle of one line, the logical value of TP is set to H to the same timing as this, and the closing motion control signal SH corresponding to the data latch

control signal TP is acquired by the output terminal of the AND gate 38.
[0810] When the alternating current-ized signal REV is reversed from a logical value H to L, it is, the output SWb, i.e., the change-over control signal, of this reversal event to the AND gate 44. It is set to L. On the other hand, when the data latch control signal TP starts on H level at the time of reversal of REV, while H level is served as, the output SH, i.e., the closing motion control signal, of the AND gate 38, and this closing motion control signal SH is activated by H level, it is, the output SWa, i.e., the change-over control signal, of the OR gate 40. It is set to H. In this way, the logical value of a change-over control signal [SWa and SWb] is set to [H, L], it sets in each 2nd change-over circuits 24L and 24R, and they are both the transfer gate TGa and TGb. Both become off. Thereby, all of both the output amplifier 22L and 22R are intercepted from the output pads 26L and 26R.
[0820] And since the closing motion control signal SH is H level, an open/close switch 30 closes, and it is the ****** signal line Xj and Xj+1. Comrades connect too hastily mutually, among both signal lines, the potentials of reversed polarity negate each other and they are equalized.
[0830] If the data latch control signal TP falls to L level, it will fall to L level, the output SH, i.e., the closing motion control signal, of the AND gate 38, and an open/close switch 30 will return to the open condition at the time of a stationary. Moreover, it is by the closing motion control signal SH falling to L level, the output SWb, i.e., the change-over control signal, of the OR gate 40. It is set to L. In this way, a change-over control signal [SWa and SWb] is set to [L, L], and it sets in each 2nd change-over circuits 24L and 24R, and is the left-hand side transfer gate TGa. By ON, it is the right-hand side transfer gate TGb. It becomes off.
[0840] As well as the above when the alternating current-ized signal REV is reversed from a logical value L to H, the 2nd change-over circuits 24L and 24R intercept temporarily at the time of the reversal, an open/close switch 30 flows in the meantime, and it is both the signal lines Xj and Xj+1. It connects too hastily mutually. It sets immediately after that in each 2nd change-over circuits 24L and 24R, and is the left-hand side transfer gate TGa. It is off and is the right-hand side transfer gate TGb. It becomes ON.
[0850] The example of a configuration of the signal-line driver by another example of this invention is shown in drawing 6 . An open/close switch 30 is connected between all ****** output pads or signal lines, and all the open/close switches 30 are made into a closed state all at once at the time of the polarity reversals of alternating-current-izing, and it constitutes from this signal-line driver so that all the signal lines X1, X2, and .... may be short-circuited mutually. In this case, between all the signal lines X1, X2, and ...., the potential of straight polarity and the potential of negative polarity negate each other, and are equalized, and the potential of each signal line X1, X2, and .. is the medium level VCOM. It converges near.
[0860] Furthermore, in this signal-line driver, an open/close switch 46 is minded for the output pad (OUTn) of an end, and it is the counterelectrode electrical potential difference VCOM. Or it has connected with the supply voltage terminal which supplies the electrical potential difference near this. This open/close switch 46 is preferably closed with the control signal SC from the change-over control circuit 32 at the back of this period during the period when all the open/close switches 30 are closed states all at once. By this, it is the counterelectrode electrical potential difference VCOM. Or the electrical potential difference near this is supplied to all the signal lines X1, X2, and .... through the switch 46 of a closed state and 30 and 30, and --. Consequently, it is the medium level VCOM at the precision with high potential of each signal line X1, X2, and .... It is reset near.
[0870] The example of circuitry of the important section of the signal-line driver by other examples is shown in drawing 7 . The actuator of each channel is made to become independent to parallel in this signal-line driver. Therefore, the change-over circuits [as / in drawing 1 and the example of a configuration of drawing 6] 14 and 24 are not formed. however, the DA converter of each channel -- the gradation electrical-potential-difference generating circuit 28 -- the whole floor tone of straight polarity -- it operates so that one gradation electrical potential difference may be chosen and electrical-potential-difference V1 -V64 and whole floor tone electrical-potential-difference V64of negative polarity' - V1' may be outputted from reception and its inside. Moreover, the output amplifier 22 of each channel is

equipped with both the functions of a sink and the source, and operates by turns in the electrical-potential-difference range of straight polarity, and the electrical-potential-difference range of negative polarity.

[0880] Although the open/close switch 30 is connected between the channels of a ****** couple in the example of a configuration of drawing 7 , an open/close switch 30 may be formed between [all] channels like drawing 6 .

[0890] In addition, in drawing 1 , drawing 6 , and drawing 7 , although the DA converter [20L 20R, and 20] is written, respectively, these are decoder circuits substantially, mean that digital data is changed into analog voltage, and are taken as the DA converter.

[0900]

[Effect of the Invention] As explained above, according to the signal-line actuation circuit for liquid crystal displays of this invention In dot reversal actuation of the common fixed driving method, short-circuit ****** signal lines temporarily at the time of the polarity reversals of alternating-current-izing, make each potential negate mutually, and it equalizes near medium level. Since it was made to drive from this equalized potential to the gradation electrical potential difference of a request of each signal line, the burden of an actuator can be mitigated and power consumption can be reduced substantially.

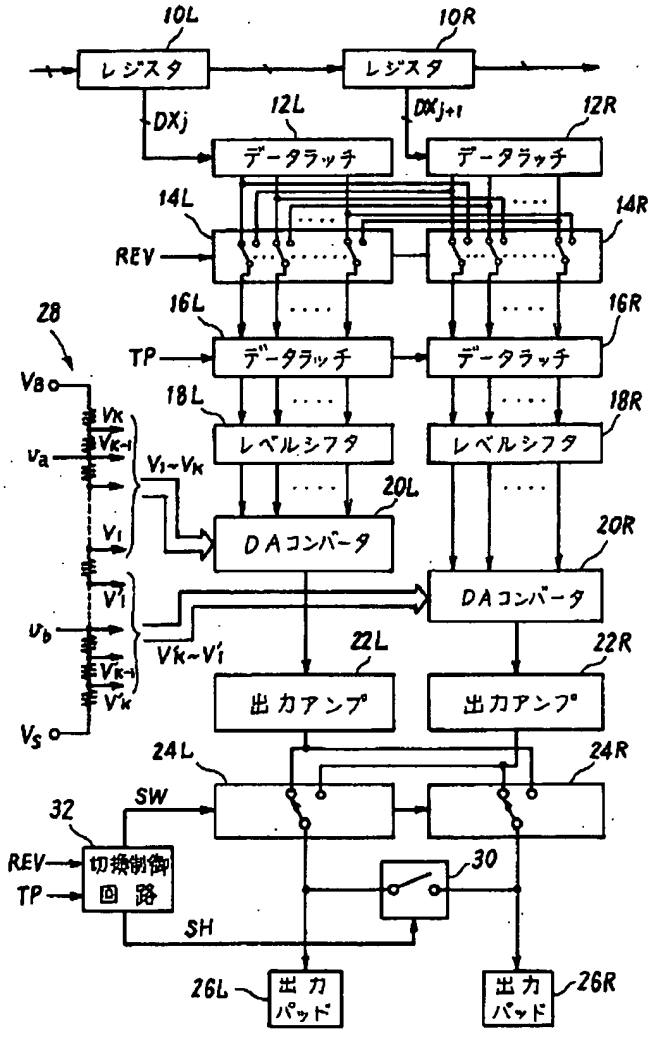
[Translation done.]

* NOTICES *

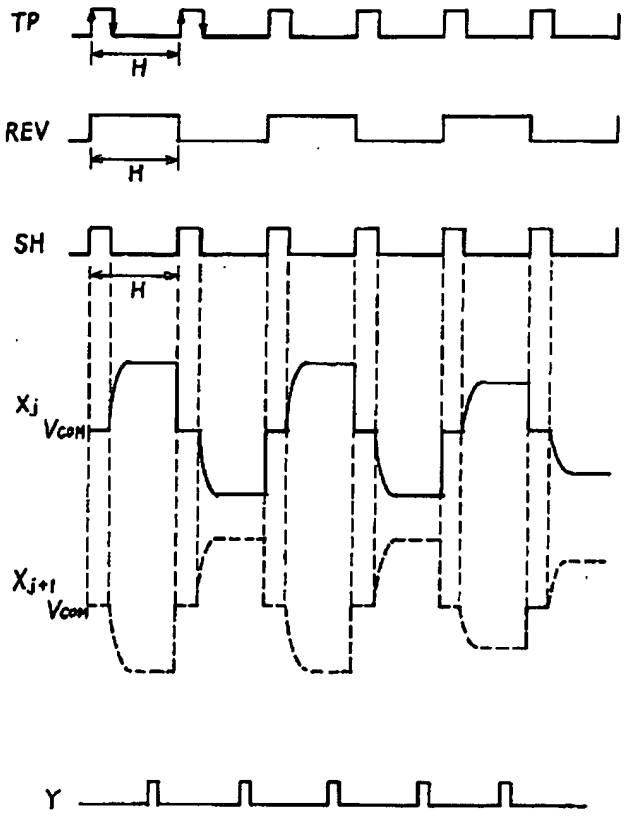
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

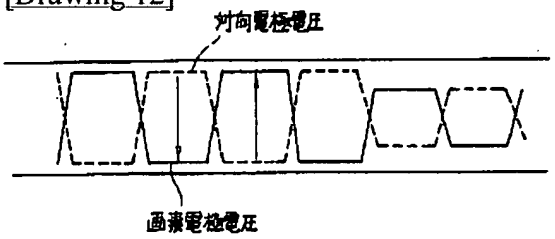
[Drawing 1]



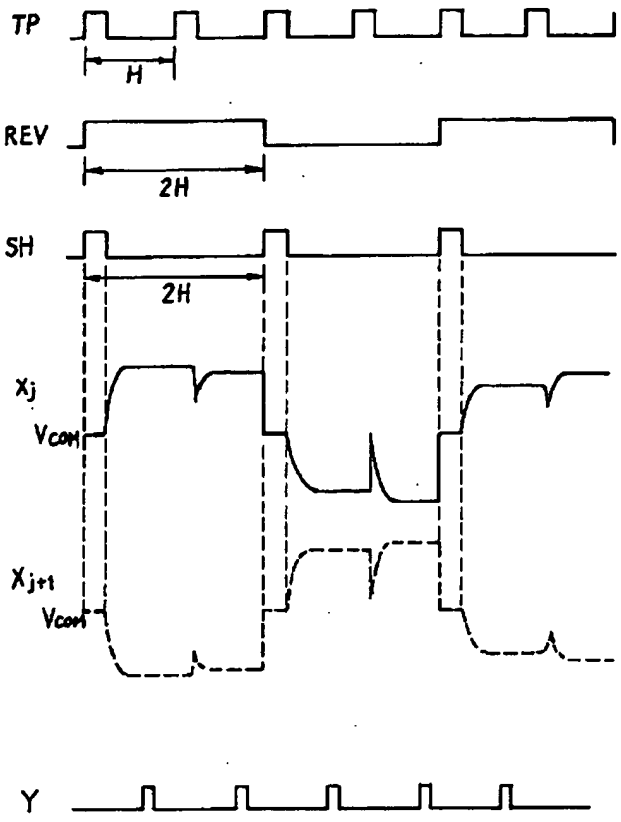
[Drawing 2]



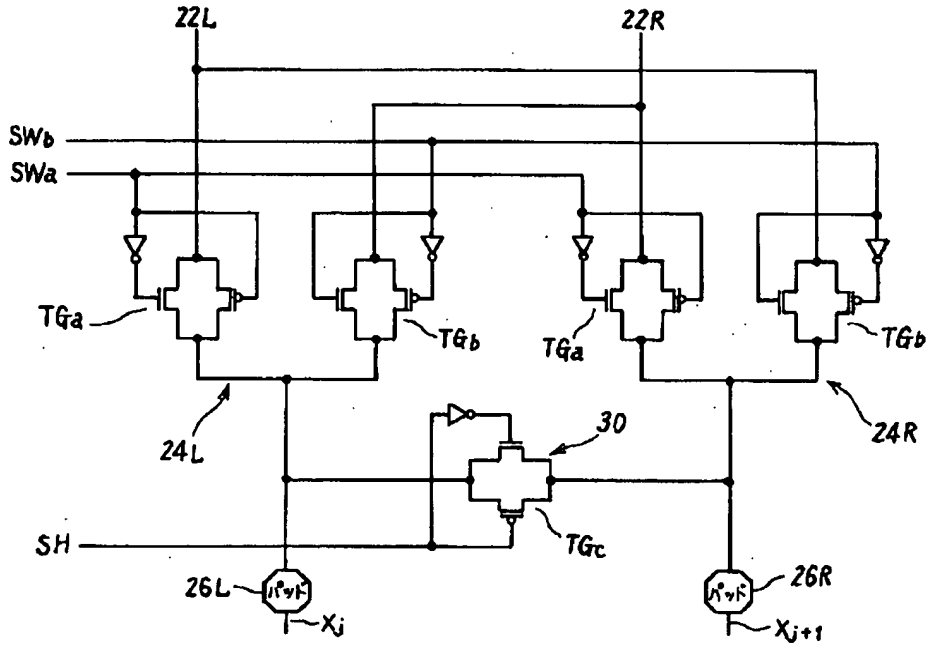
[Drawing 12]



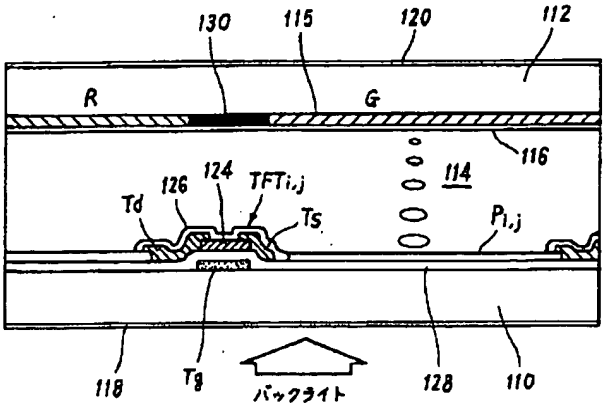
[Drawing 3]



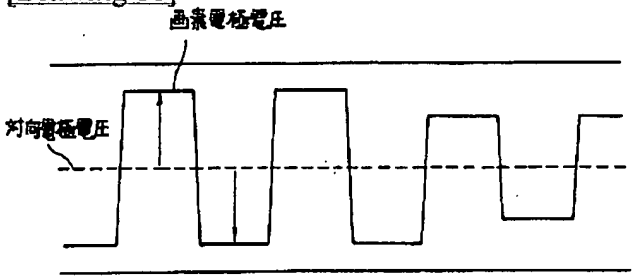
[Drawing 4]



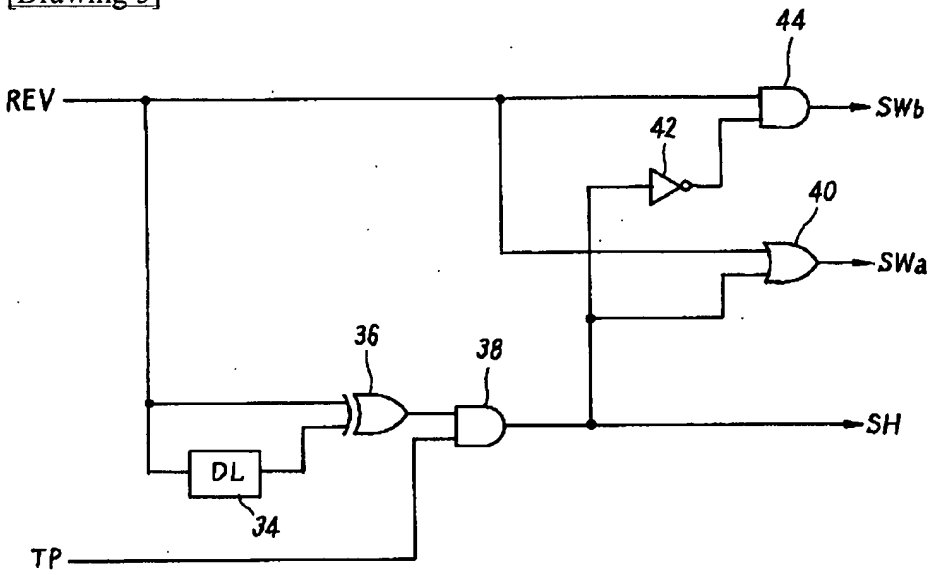
[Drawing 9]



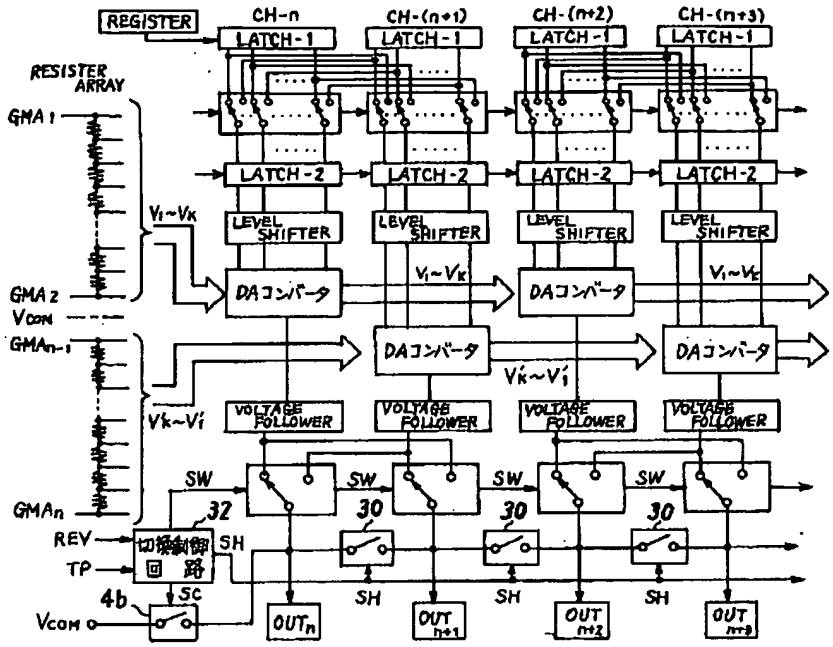
[Drawing 11]



[Drawing 5]

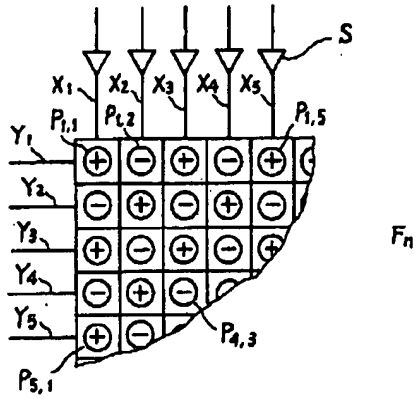


[Drawing 6]



[Drawing 13]

(A)



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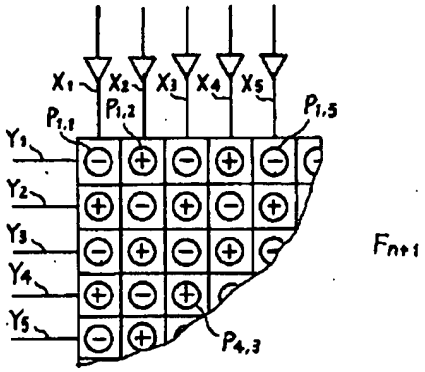
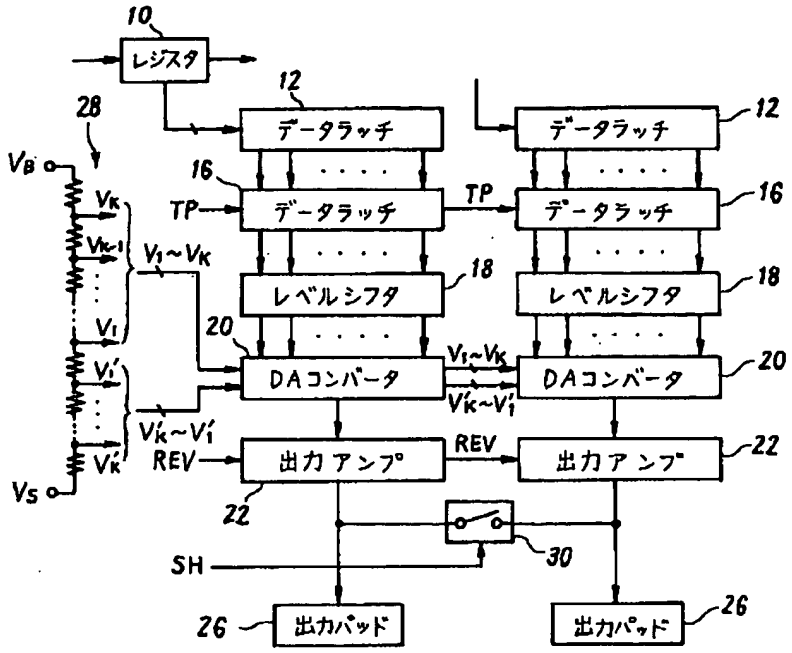
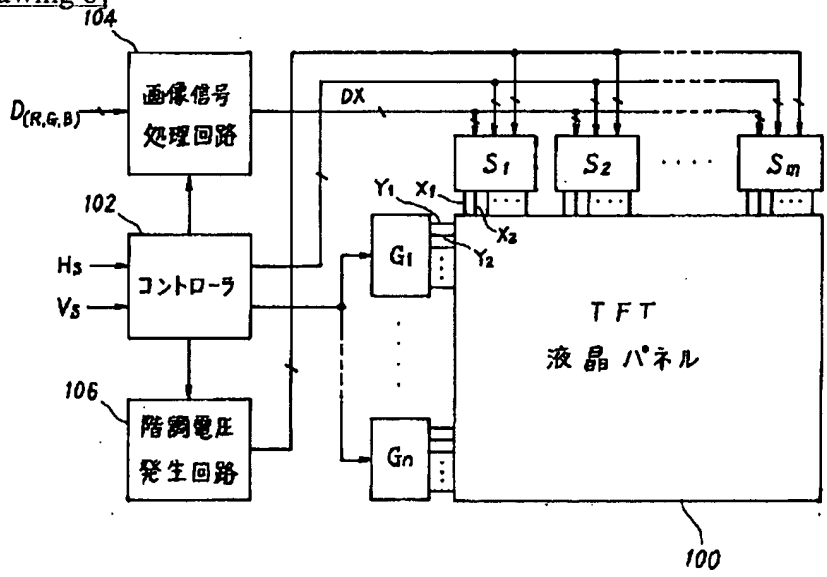


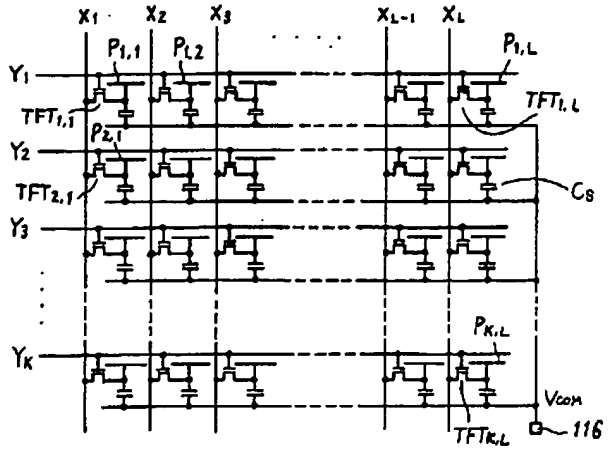
[Drawing 7]



[Drawing 8]



[Drawing 10]



[Translation done.]